Monte Carlo Study of Stacking Fault Interactions during 3C-SiC Epitaxial Growth

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3C-SiC has emerged as an attractive wide bandgap semiconducting material for high temperature, high frequency, and high voltage applications. It exhibits a low density of states at the 3C-SiC/SiO₂ interface, making it a viable material for power-switching MOSFETs which are of particular interest to motor drives in electric vehicles. Moreover, 3C-SiC can be grown on a Si substrate to drive down production costs. However, as a result of the 19.7% lattice mismatch between Si and 3C-SiC, a high density of stacking faults are generated and a specific interaction between adjoining stacking faults generates an electrically active defect which can degrade the performance of 3C-SiC devices. Here we employ Monte Carlo simulations to better understand the interaction of stacking faults during epitaxial growth of 3C-SiC on a Si substrate. By modeling the generation, annihilation, and termination of stacking faults in 3C-SiC grown on the Si(100) face as well as the Si(111) face, we can compare the densities of stacking faults and electrically active defects for both geometries. For both cases, we monitored the evolution of defect density as a function of 3C-SiC film thickness for various different sizes of crystals ranging from 15×15 μm² to 1000×1000 μm². In contrast to that of (100)-oriented 3C-SiC, the stacking faults on the (111) face have unified polarities which gives rise to increased annihilation. Therefore, we expect to see that the stacking fault density will decrease more rapidly in the case of (111)-oriented 3C-SiC growth.



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} (-111)

--- 15 μm x15 μm

60 80 100 120 140 160 180 200

SiC Thickness (µm)

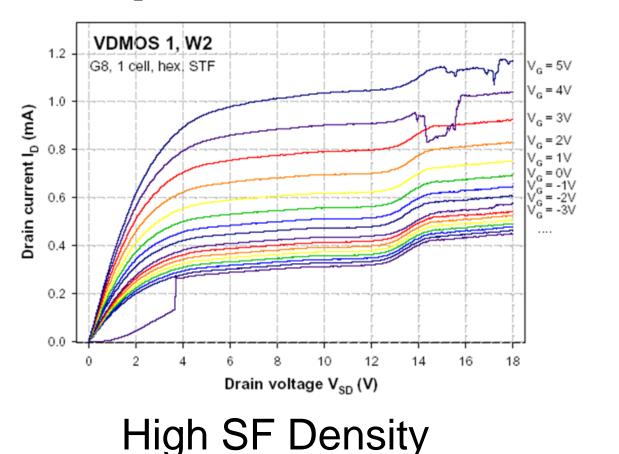
-- 30 μm x30 μm

— 90 μm x90 μm

-150 μm x150 μm

Motivation

3C-SiC shows promise for use in high temperature, high voltage, and high frequency power switching devices. However, large stacking fault densities within the crystal can degrade electrical properties. Therefore, it is important to study stacking fault interactions during epitaxial growth so that defect reduction can be optimized.



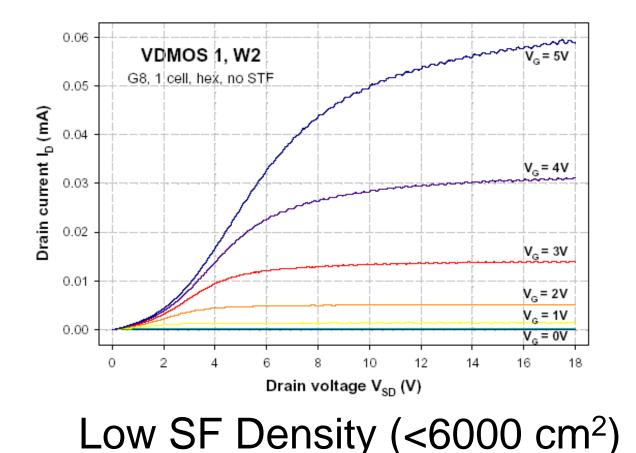


Figure 1: Plots of drain current versus drain voltage for power MOSFETs synthesized from 3C-SiC¹

Goal: Monitor stacking fault density reduction during epitaxial growth for various crystal sizes and orientations

Stacking Faults (SFs) in 3C-SiC

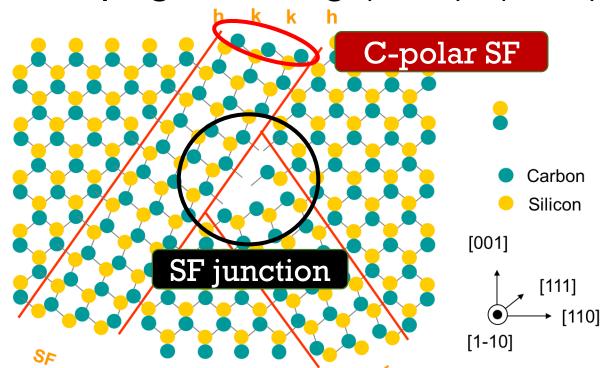
- SFs are generated at the interface between the 3C-SiC crystal and Si substrate during epitaxial growth in order to minimize the incoherence generated by the 19.7% lattice mismatch
- SFs propagate along the four equivalent {111} planes of 3C-SiC

3C-SiC(001) Face

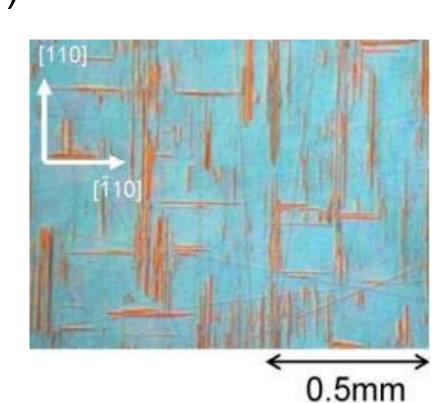
- 4 Orientations of SFs expressed:
- 2 with Carbon Polarity
- 2 with Silicon Polarity
- C polar and Si polar SFs are related by 90° rotations

3C-SiC(111) Face

- 3 Orientations of SFs expressed:
- All have unified polarity
- Propagate along (11-1), (1-11), and (-111)







SF Interactions:

SFs with like polarity: one

SFs with <u>distinct</u> polarity:

each terminate the other's

Point defects at SF

junctions can introduce

states into the band gap

will annihilate the other

propagation

Figure 3. 3C-SiC surface after KOH etching to accentuate SFs³

Monte Carlo Simulation Geometry of Simulation Setup: 3C-SiC(001) 3C-SiC(111) **(11-1)** Si-polar SFs **(1-11) Evolution of a SF Interaction Simulation:** SiC Thickness = $0.872 \mu m$ SiC Thickness = $5.232 \mu m$ **Initial Carbonization** SF Density = $2.4x10^5$ /cm SF Density = $4.57x10^4$ /cm **Summary of Stacking Fault Interactions⁴:** Interactive shrinking mode Self expansion mode Drag mode Self shrinking mode Interactive stretching mode Annihilation mode **Key Simulation Parameters:** 12.5% (for Si-Static Generation Expansion Probability polar SFs) Probability for SFs Annihilation Balance Angle Offset

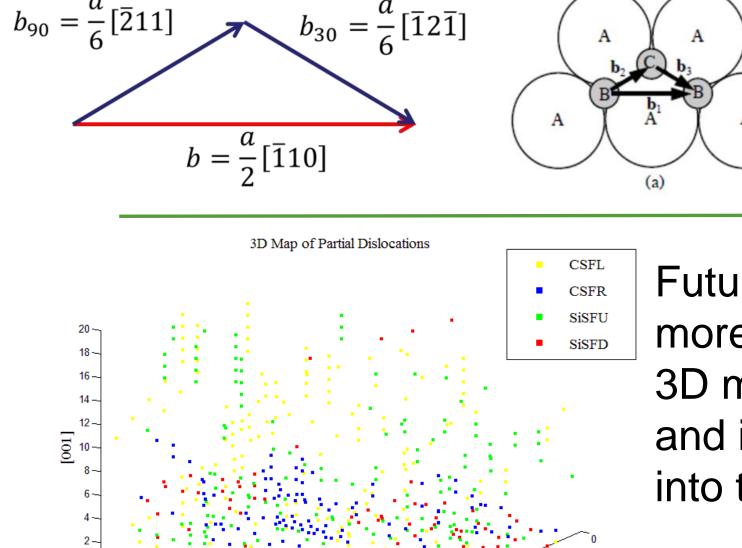
Dislocation (SF Edge) Density Reduction - 30 μm x30 μm → 30 μm x30 μm -90 μm x90 μm - 90 μm x90 μm Comparison between (001) and (111) Face

Conclusion

- SF density decreases with increasing thickness and decreasing crystal area size on both the 3C-SiC(001) and the 3C-SiC(111) surfaces as a result of annihilation and termination interactions
- At some specific thickness, determined by area size, stacking fault density decreases dramatically
- Stacking fault density decreases more rapidly on the (111) face than the (001) face

Future Work

Depending on the polarity, SFs in 3C-SiC may be terminated by Shockley-type partial dislocations which can glide and interact along the four equivalent {111} planes. The glide of dislocations can change the dimensions of the stacking fault. Figure 4. SFs are



bordered by 30° and 90° partial dislocations which glide parallel to their Burger's vectors⁵

Future simulations can be made more comprehensive by employing 3D mapping of partial dislocations and incorporating dislocation glide into the algorithm.

Figure 5. 3D map of dislocations during simulation on 3C-SiC(001)

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Stacking Fault Density Reduction

→ 15 μm x15 μm

SiC Thickness (μm)

— 30 μm x30 μm

-90 μm x90 μm

150 μm x150 μm

References

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